

IN THE SPECIFICATION:

Please replace paragraph number [0001] with the following rewritten paragraph:

[0001] This application is a continuation of application Serial No. 09/941,092, filed August 28, 2001, ~~pending,~~ now U.S. Patent 6,373,011, issued April 16, 2002, which is a continuation of application Serial No. 09/713,912, filed November 15, 2000, ~~pending,~~ now U.S. Patent 6,365,861, issued April 2, 2002, which is a division of application Serial No. 09/520,067, filed March 7, 2000, now U.S. Patent 6,350,959 B1, issued February 26, 2002, which is a continuation of application Serial No. 09/133,338, filed August 13, 1998, now U.S. Patent 6,100,486, issued August 8, 2000, which is a division of application Serial No. 08/785,353, filed January 17, 1997, now U.S. Patent 5,927,512, issued July 27, 1999.

Please replace paragraph number [0002] with the following rewritten paragraph:

[0002] The present application is also related to: application Serial No. 08/591,238, filed January 17, 1996, now abandoned; application Serial No. 08/664,109, filed June 13, 1996, now U.S. Patent 5,895,962, issued April 20, 1999; a divisional application having Serial No. 09/133,336, filed August 13, 1998, now U.S. Patent 6,147,316, issued November 14, 2000; a ~~co-~~ ~~pending~~ co-pending application having Serial No. 08/822,731, filed March 24, 1997, now U.S. Patent 5,856,923, issued January 5, 1999; a co-pending application having Serial No. 08/806,442, filed February 26, 1997, now U.S. Patent 5,915,231, issued June 22, 1999; a co-pending application having Serial No. 08/871,015, filed June 6, 1997, now U.S. Patent 5,907,492, issued May 25, 1999; and a co-pending application having Serial No. 08/801,565 filed February 17, 1997, now U.S. Patent 5,844,803, issued December 1, 1998.

Please replace paragraph number [0003] with the following rewritten paragraph:

[0003] Field of the Invention: The present invention relates in general to integrated circuit (IC) manufacturing and, more specifically, to methods in IC manufacturing processes for sorting IC devices using identification (ID) codes, such as fuse ~~ID's,~~ IDs, in the devices.

Please replace paragraph number [0004] with the following rewritten paragraph:

[0004] State of the Art: Integrated circuits (~~IC's~~) (ICs) are small electronic circuits formed on the surface of a wafer of semiconductor material, such as silicon, in an IC manufacturing process referred to as "fabrication." Once fabricated, ~~IC's~~ ICs are electronically probed to evaluate a variety of their electronic characteristics, cut from the wafer on which they were formed into discrete IC dice or "chips," and then assembled for customer use using various well-known IC packaging techniques, including lead frame packaging, Chip-On-Board (COB) packaging, and flip-chip packaging.

Please replace paragraph number [0005] with the following rewritten paragraph:

[0005] Before being shipped to customers, packaged ~~IC's~~ ICs are generally tested to ensure they will function properly once shipped. Testing typically involves a variety of known test steps, such as pre-grade, burn-in, and final, which test ~~IC's~~ ICs for defects and functionality and grade ~~IC's~~ ICs for speed. As shown in FIG. 1, ~~IC's~~ ICs that pass the described testing are generally shipped to customers, while ~~IC's~~ ICs that fail the testing are typically rejected.

Please replace paragraph number [0006] with the following rewritten paragraph:

[0006] The testing standards for a particular IC product are sometimes relaxed as the product "~~matures~~" "matures," such that ~~IC's~~ ICs previously rejected under strict testing standards may pass the relaxed testing standards. Consequently, reject bins containing previously rejected ~~IC's~~ ICs are sometimes "culled" for ~~IC's~~ ICs that are shippable under relaxed testing standards by testing the rejected ~~IC's~~ ICs again using the relaxed testing standards. Unfortunately, while this "~~culling~~" culling process does retrieve shippable ~~IC's~~ ICs from reject bins, it makes inefficient use of expensive and often limited testing resources by diverting those resources away from testing untested ~~IC's~~ ICs in order to retest previously rejected ~~IC's~~ ICs. Therefore, there is a need in the art for an improved method of "~~culling~~" culling or sorting such reject bins for shippable ~~IC's~~ ICs.

Please replace paragraph number [0007] with the following rewritten paragraph:

[0007] Similarly, as shown in FIG. 2, all the ~~IC's~~ ICs from the wafers in a wafer lot typically undergo enhanced reliability testing that is more extensive and strict than normal testing when any of the wafers in the lot are deemed to be unreliable because of fabrication or other process errors. Since a wafer lot typically consists of ~~fifty~~ 50 or more wafers, many of the ~~IC's~~ ICs that undergo the enhanced reliability testing do not require it because they come from wafers that are not deemed unreliable. Performing enhanced reliability testing on ~~IC's~~ ICs that do not need it is inefficient because such testing is typically more time-consuming and uses more resources than normal testing. Therefore, there is a need in the art for a method of sorting ~~IC's~~ ICs from a wafer lot into those ~~IC's~~ ICs that require enhanced reliability testing and those that do not.

Please replace paragraph number [0008] with the following rewritten paragraph:

[0008] Likewise, as shown in FIG. 3, a new or special "recipe" for fabricating ~~IC's~~ ICs on wafers is sometimes tested by fabricating some wafers from a wafer lot using the special recipe and other wafers from the wafer lot using a control recipe. ~~IC's~~ ICs from the wafers then typically undergo separate assembly and test procedures so that the test results of ~~IC's~~ ICs fabricated using the special recipe are not mixed with the test results of ~~IC's~~ ICs fabricated using the control recipe, and vice versa. Test reports from the separate test procedures are then used to evaluate the special recipe and to determine whether the ~~IC's~~ ICs are to be shipped to customers, reworked, repaired, retested, or rejected. Unfortunately, because the ~~IC's~~ ICs undergo separate test and assembly procedures, undesirable variables, such as differences in assembly and test equipment, are introduced into the testing of the special recipe. It would be desirable, instead, to be able to assemble and test the ~~IC's~~ ICs using the same assembly and test procedures, and to then sort the ~~IC's~~ ICs and their test results into those ~~IC's~~ ICs fabricated using the special recipe and those ~~IC's~~ ICs fabricated using the control recipe. Therefore, there is a need in the art for a method of identifying individual ~~IC's~~ ICs fabricated using a special or control recipe and sorting the ~~IC's~~ ICs based on their fabrication recipe.

Please replace paragraph number [0009] with the following rewritten paragraph:

[0009] As described above, ~~IC's~~ ICs are typically tested for various characteristics before being shipped to customers. For example, as shown in FIG. 4, ~~IC's~~ ICs may be graded in test for speed and placed in various bins (e.g., 5 nanoseconds (ns), 6ns, and 7ns bins) according to their grading. If a customer subsequently requests a more stringent speed grade (e.g., 4ns), ~~IC's~~ ICs in one of the bins (e.g., a 5ns bin) are ~~re-tested~~ retested and thereby sorted into ~~IC's~~ ICs that meet the more stringent speed grade (e.g., 4ns bin) and those that do not (e.g., 5ns bin). While this conventional process sorts the ~~IC's~~ ICs into separate speed grades, it makes inefficient use of expensive and often limited testing resources by diverting those resources away from testing untested ~~IC's~~ ICs in order to retest previously tested ~~IC's~~ ICs. Therefore, there is a need in the art for an improved method of "~~culling~~" culling or sorting bins for ~~IC's~~ ICs that meet more stringent standards, such as a higher speed grading.

Please replace paragraph number [0010] with the following rewritten paragraph:

[0010] As described in U.S. Patent ~~No.'s~~ Nos. 5,301,143, 5,294,812, and 5,103,166, some methods have been devised to electronically identify individual ~~IC's~~ ICs. Such methods take place "off" the manufacturing line and involve the use of electrically retrievable ID codes, such as ~~so-called~~ so-called "fuse ~~ID's~~" IDs," programmed into individual ~~IC's~~ ICs to identify the ~~IC's~~ ICs. The programming of a fuse ID typically involves selectively blowing an arrangement of fuses and anti-fuses in an IC so that when the fuses or anti-fuses are accessed, they output a selected ID code. Unfortunately, none of these methods addresses the problem of identifying and sorting ~~IC's~~ ICs "on" a manufacturing line.

Please replace paragraph number [0011] with the following rewritten paragraph:

[0011] An inventive method for sorting integrated circuit (IC) devices of the type to have a substantially unique identification (ID) code, such as a fuse ID, ~~includes~~ including automatically reading the ID code of each of the IC devices and sorting the IC devices according to their automatically read ID codes. The inventive method can be used in conjunction with an

IC manufacturing process that includes providing semiconductor wafers, fabricating the ~~IC's~~ ICs on each of the wafers, causing each of the ~~IC's~~ ICs to store its ID code, separating each of the ~~IC's~~ ICs from its wafer to form an IC die, assembling the IC dice into IC devices, and testing the IC devices. The method can also be used in conjunction with Single In-line Memory Module (SIMM), Dual In-line Memory Module (DIMM), and other multi-chip module (MCM) manufacturing processes.

Please replace paragraph number [0014] with the following rewritten paragraph:

[0014] In still another embodiment, a method for sorting a group of IC devices in accordance with a first IC standard, such as a speed standard, that have previously been sorted in accordance with a second IC standard, such as a ~~speed-standard~~ standard, that is less stringent than the first IC standard, includes storing test results that caused each of the IC devices in the group to be sorted into the group in connection with ID codes, such as fuse-~~ID's~~, IDs, of the devices, automatically reading the ID code from each of the IC devices, accessing the test results stored in connection with each of the automatically read ID codes, comparing the accessed test results for each of the IC devices with the first IC standard, and sorting the IC devices according to whether their test results pass the first IC standard.

Please replace paragraph number [0016] with the following rewritten paragraph:

[0016] Thus, the inventive method described above provides an advantageous method for sorting ~~IC's~~ ICs from the same wafer lot into those ~~IC's~~ ICs that require enhanced reliability testing and those that do not.

Please replace paragraph number [0017] with the following rewritten paragraph:

[0017] In a still further embodiment, an inventive method in an IC manufacturing process for testing different fabrication process recipes includes the following: providing first and second pluralities of semiconductor wafers; fabricating a first plurality of ~~IC's~~ ICs on each of the first plurality of wafers in accordance with a control recipe; fabricating a second plurality

of ~~IC's~~ ICs on each of the second plurality of wafers in accordance with a test recipe; causing each of the ~~IC's~~ ICs on each of the wafers to permanently store a substantially unique ID code, such as a fuse ID; separating each of the ~~IC's~~ ICs on each of the wafers from its wafer to form one of a plurality of IC dice; assembling each of the IC dice into an IC device; automatically reading the ID code from the IC in each of the IC devices; testing each of the IC devices; and sorting each of the IC devices in accordance with the automatically read ID code from the IC in each of the IC devices indicating the IC is from one of the first and second pluralities of ~~IC's~~ ICs.

Please replace paragraph number [0018] with the following rewritten paragraph:

[0018] FIG. 1 is a flow diagram illustrating a conventional procedure in an integrated circuit (IC) manufacturing process for culling shippable ~~IC's~~ ICs from a reject bin;

Please replace paragraph number [0019] with the following rewritten paragraph:

[0019] FIG. 2 is a flow diagram illustrating a conventional procedure in an IC manufacturing process for directing ~~IC's~~ ICs to enhanced reliability testing;

Please replace paragraph number [0021] with the following rewritten paragraph:

[0021] FIG. 4 is a flow diagram illustrating a conventional procedure in an IC manufacturing process for speed-sorting ~~IC's~~ ICs;

Please replace paragraph number [0022] with the following rewritten paragraph:

[0022] FIG. 5 is a flow diagram illustrating a procedure in an integrated circuit (IC) manufacturing process for culling shippable ~~IC's~~ ICs from a reject bin in accordance with the present invention;

Please replace paragraph number [0023] with the following rewritten paragraph:

[0023] FIG. 6 is a flow diagram illustrating a procedure in an IC manufacturing process for directing ~~IC's~~ ICs to enhanced reliability testing in accordance with another embodiment of the present invention;

Please replace paragraph number [0025] with the following rewritten paragraph:

[0025] FIG. 8 is a flow diagram illustrating a procedure in an IC manufacturing process for speed-sorting ~~IC's~~ ICs in accordance with a further embodiment of the present invention.

Please replace paragraph number [0026] with the following rewritten paragraph:

[0026] As shown in FIG. 5, an inventive method for sorting integrated circuit (IC) devices is embodied in a method 10 in an IC manufacturing process for culling shippable ~~IC's~~ ICs from a reject bin 12. It will be understood by those having skill in the field of this invention that the present invention is applicable to sorting any IC devices, including Dynamic Random Access Memory (DRAM) ~~IC's~~, ICs, Static Random Access Memory (SRAM) ~~IC's~~, ICs, Synchronous DRAM (SDRAM) ~~IC's~~, ICs, processor ~~IC's~~, ICs, Single In-line Memory Modules (~~SIMM's~~), (SIMMs), Dual In-line Memory Modules (~~DIMM's~~), (DIMMs), and other Multi-Chip Modules (~~MCM's~~), (MCMs).

Please replace paragraph number [0027] with the following rewritten paragraph:

[0027] The method 10 includes the step of fabricating 14 ~~of fabricating IC's~~ ICs on wafers from a wafer lot 16. ~~IC's~~ ICs fabricated on the wafers are then programmed in a program step 18 in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID may identify a wafer lot ID, the week the ~~IC's~~ ICs were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID. It will be understood, of course, that the present invention includes within its scope ~~IC's~~ ICs having any ID code, including those having fuse ~~ID's~~, IDs. It will also be understood that the ID code for each IC need not be unique, but instead may only specify the wafer the IC comes from, for example.

Please replace paragraph number [0028] with the following rewritten paragraph:

[0028] Once programmed, the ~~IC's~~ ICs proceed through an assembly step 20 to a test step 22 where the fuse ~~ID's~~ IDs are automatically read and stored in association with test data 24 generated in the test step 22. Although the fuse ~~ID's~~ IDs are typically read electronically, it will be understood that they may also be read optically if the fuse ID consists of "blown" laser fuses that are optically accessible. It will also be understood that the test data 24 may include data such as the following: data identifying the testing equipment that tested the ~~IC's~~, ICs, operating personnel who operated the testing equipment, and the set-up of the equipment when the ~~IC's~~ ICs were tested; and data indicating the time and date the ~~IC's~~ ICs were tested, the yield of shippable ~~IC's~~ ICs through the test step 22, and test results for the ~~IC's~~ ICs from the various stages of the test step 22.

Please replace paragraph number [0029] with the following rewritten paragraph:

[0029] ~~IC's~~ ICs that pass the test step 22 are typically shipped to customers, while those that fail the test step 22 are directed to the reject bin 12. At a point in time when test standards of the test step 22 have been relaxed as described above, the ~~IC's~~ ICs in the reject bin 12 are sorted in a sort step 26 by reading the fuse ID of each IC, accessing the test data 24 associated with the fuse ID, and comparing the accessed test data 24 with the relaxed test standards. Those ~~IC's~~ ICs that fail even the relaxed test standards are directed back to the reject bin 12, while those ~~IC's~~ ICs that pass the relaxed test standards are typically shipped to customers. The method 10 thus successfully culls shippable ~~IC's~~ ICs from the reject bin 12 without retesting the ~~IC's~~ ICs.

Please replace paragraph number [0030] with the following rewritten paragraph:

[0030] As shown in FIG. 6, the inventive sorting method is also embodied in a ~~back-end~~ back-end (i.e., after fabrication) test method 30 for separating ~~IC's~~ ICs in need of enhanced reliability testing from a group of ~~IC's~~ ICs undergoing back-end test procedures. ~~IC's~~ ICs typically require enhanced reliability testing because the wafer they come from is unreliable as a result of fabrication errors and other unintended manufacturing process deviations.



Please replace paragraph number [0031] with the following rewritten paragraph:

[0031] The method 30 includes the step 32 of fabricating ~~IC's~~ ICs on wafers from a wafer lot 34. ~~IC's~~ ICs fabricated on the wafers are then programmed in a program step 36 in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID may identify a wafer lot ID, the week the ~~IC's~~ ICs were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID. It will be understood, of course, that the present invention includes within its scope ~~IC's~~ ICs having any ID code, including those having fuse ~~ID's~~ IDs. It will also be understood that the ID code for each IC need not be unique, but instead may only specify the wafer the IC comes from, for example.

Please replace paragraph number [0032] with the following rewritten paragraph:

[0032] Once programmed, the ~~IC's~~ ICs proceed through an assembly step 38. At this point in the IC manufacturing process, it is not uncommon for a number of wafers to have been identified as being unreliable for the reasons stated above. The fuse ~~ID's~~ IDs of the ~~IC's~~ ICs that come from these unreliable wafers may then be associated with a stored flag indicating the ~~IC's~~ ICs come from unreliable wafers. If any wafers in the wafer lot 34 have been identified as being unreliable, the ~~IC's~~ ICs proceed to a sort step 40, where their fuse ~~ID's~~ IDs are automatically read so the ~~IC's~~ ICs can be sorted into those flagged as coming from the unreliable wafers that require processing through an enhanced reliability testing step 42 and those not flagged as coming from the unreliable wafers that may proceed through a standard test step 44. Of course, those ~~IC's~~ ICs that pass either the standard test step 44 or the enhanced reliability testing step 42 are typically shipped to customers, while those that fail these steps are directed to a reject bin (not shown).

Please replace paragraph number [0033] with the following rewritten paragraph:

[0033] Thus, the present invention provides a method 30 that directs those ~~IC's~~ ICs needing enhanced reliability testing to the enhanced reliability testing ~~step 42~~ step 42, while

allowing those that do not require enhanced reliability testing to proceed through the standard testing step 44.

Please replace paragraph number [0035] with the following rewritten paragraph:

[0035] The method 50 includes fabricating some of the wafers from a wafer lot 52 in a fabrication step 54 in accordance with a control process recipe that is typically the normal process recipe in use in the IC manufacturing process at the time. The remainder of the wafers from the wafer lot 52 ~~are~~ is fabricated in another fabrication step 56 in accordance with a special or test process recipe. The special or test process recipe may change a variety of variables in the fabrication process, including doping, the thickness of IC layers, etc.

Please replace paragraph number [0036] with the following rewritten paragraph:

[0036] Once the ~~IC's~~ ICs are fabricated in the fabrication steps 54 and 56, the ~~IC's~~ ICs are then programmed in a program step 58 in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID may identify a wafer lot ID, the week the ~~IC's~~ ICs were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID. It will be understood, of course, that the present invention includes within its scope ~~IC's~~ ICs having any ID code, including those having fuse ~~ID's~~ IDs. It will also be understood that the ID code for each IC need not be unique, but instead may only specify the wafer the IC comes from, for example.

Please replace paragraph number [0037] with the following rewritten paragraph:

[0037] Once programmed, the ~~IC's~~ ICs proceed through an assembly step 60 to a test step 62 where the fuse ~~ID's~~ IDs are automatically read and stored in association with test data 64 generated for both the control recipe ~~IC's~~ ICs and the special or test recipe ~~IC's~~ ICs in the test step 62. Although the fuse ~~ID's~~ IDs are typically read electronically, it will be understood that they may also be read optically if the fuse ID consists of "blown" laser fuses that are optically accessible. It will also be understood that the test data 64 may include data such as the

following: data identifying the testing equipment that tested the ~~IC's~~, ICs, operating personnel who operated the testing equipment, and the set-up of the equipment when the ~~IC's~~ ICs were tested; and data indicating the time and date the ~~IC's~~ ICs were tested, the yield of shippable ~~IC's~~ ICs through the test step 62, and test results for the ~~IC's~~ ICs from the various stages of the test step 62.

Please replace paragraph number [0038] with the following rewritten paragraph:

[0038] Once the test data 64 is generated, the data 64 may be analyzed 67 to determine those ~~IC's~~ ICs that are shippable and those that are not, and to determine any differences in test results between the control recipe ~~IC's~~ ICs and the special or test recipe ~~IC's~~ ICs. The ~~IC's~~ ICs are sorted in a sort step 66 so they may be shipped, reworked, repaired, retested, or rejected in accordance with the analysis of the test results.

Please replace paragraph number [0039] with the following rewritten paragraph:

[0039] By sorting the control recipe 68 and special or test recipe 69 ~~IC's~~ ICs at the end of the IC manufacturing process, the method 50 is able to assemble and test the ~~IC's~~ ICs together and thus eliminate unintended variables introduced into the process of testing the special or test recipe by the conventional method of assembling and testing the ~~IC's~~ ICs separately. The inventive method 50 thus provides more reliable test results.

Please replace paragraph number [0040] with the following rewritten paragraph:

[0040] As shown in FIG. 8, the inventive method for sorting IC devices is also embodied in a method 70 in an IC manufacturing process for sorting IC devices in accordance with an IC standard, such as speed, that is more stringent than an IC standard that the devices were previously sorted in accordance with. It will be understood that although the method of FIG. 8 will be described with respect to speed-sorting, the method is applicable to all situations in which ~~IC's~~ ICs previously sorted in accordance with an IC standard, such as speed, need to be sorted in accordance with another, more stringent IC standard. Such IC standards may include,

for example, access time, data setup time, data hold time, standby current, refresh current, and operating current.

Please replace paragraph number [0041] with the following rewritten paragraph:

[0041] The method 70 includes the step 72 of fabricating ~~IC's~~ ICs on wafers from a wafer lot 74. ~~IC's~~ ICs fabricated on the wafers are then programmed in a program step 76 in the manner described above with a fuse identification (ID) unique to each IC. The fuse ID may identify a wafer lot ID, the week the ~~IC's~~ ICs were fabricated, a wafer ID, a die location on the wafer, and a fabrication facility ID. It will be understood, of course, that the present invention includes within its scope ~~IC's~~ ICs having any ID code, including those having fuse ~~ID's~~ IDs.

Please replace paragraph number [0042] with the following rewritten paragraph:

[0042] Once programmed, the ~~IC's~~ ICs proceed through an assembly step 78 to a test step 80 where the fuse ~~ID's~~ IDs are automatically read and stored in association with test data 82 generated in the test step 80. Although the fuse ~~ID's~~ IDs are typically read electronically, it will be understood that they may also be read optically if the fuse ID consists of "blown" laser fuses that are optically accessible. It will also be understood that the test data 82 includes speed grading data for each IC, as described above, and may include data such as the following: data identifying the testing equipment that tested the ~~IC's~~ ICs, operating personnel who operated the testing equipment, and the set-up of the equipment when the ~~IC's~~ ICs were tested; and data indicating the time and date the ~~IC's~~ ICs were tested, the yield of shippable ~~IC's~~ ICs through the test step 80, and test results for the ~~IC's~~ ICs from the various stages of the test step 80.

Please replace paragraph number [0043] with the following rewritten paragraph:

[0043] ~~IC's~~ ICs that pass the test step 80 are typically directed to speed graded bins 84, 86, and 88, while those that fail the test step 80 are directed to a reject bin 90. The speed graded bins 84, 86, and 88 typically each contain ~~IC's~~ ICs of varying speeds. For example, the bin 88 may contain a variety of 5.0ns, 4.5ns, 4.0ns, 3.5ns, etc. parts, the bin 86 may contain a variety of

6.0ns, 5.5ns, 5.1ns, etc. parts, and the bin 84 may contain a variety of 7.0ns, 6.5ns, 6.1ns, etc. parts.

Please replace paragraph number [0044] with the following rewritten paragraph:

[0044] On occasion, customers request ~~IC's~~ ICs that meet a more stringent speed standard (e.g., 4 nanoseconds (ns)) than any of the ~~IC's~~ ICs in the various bins 84, 86, and 88 have been graded for. While bin 88, for example, may contain ~~IC's~~ ICs that will meet the more stringent speed standard, the bin 88 cannot be used to supply the customer's request because the ~~IC's~~ ICs in the bin 88 have only been graded (i.e., are guaranteed to meet or exceed) a lower speed standard (e.g., 5ns). Therefore, the present inventive method 70 sorts the ~~IC's~~ ICs in a sort step 92 by reading the fuse ID of each IC, accessing the test data 82, including the speed-grading data, associated with the fuse ID, and comparing the accessed speed-grading data with the more stringent speed standard (e.g., 4ns). Those ~~IC's~~ ICs that fail the more stringent speed standard are directed to a speed graded bin 94, while those ~~IC's~~ ICs that pass the more stringent speed standard are directed to another speed graded bin 96 where they can be used to fill the customer's request. The inventive method 70 thus sorts the ~~IC's~~ ICs in accordance with a more stringent IC standard, such as speed, than they were previously sorted in accordance with without having to retest the ~~IC's~~, ICs, and thus without reusing valuable testing resources to retest ~~IC's~~, ICs.

Please replace paragraph number [0045] with the following rewritten paragraph:

[0045] Although the present invention has been described with reference to particular embodiments, the invention is not limited to these described embodiments. For example, while the various steps of the embodiments of the inventive sorting method have been described as occurring in a particular order, it will be understood that these steps need not necessarily occur in the described order to fall within the scope of the present invention. Thus, the invention is limited only by the appended claims, which include within their ~~scope~~ scope, all equivalent methods that operate according to the principles of the invention as described.